CLAIMS

What is claimed is:

1. A synchronized parallel running power converter, controlled by a single-phase pulse-width modulator; said single-phase pulse-width modulator having a first pulse output port and a second pulse output port for pulse outputs, said power converter comprising:

a first power converter, having a first pulse input port, a second pulse input port and a current output port; said first pulse input port is coupled to said first pulse output port of said single-phase pulse-width modulator; said second pulse input port is coupled to said second pulse output port of said single-phase pulse-width modulator; and

a second power converter, having a first pulse input port, a second pulse input port and a current output port; said first pulse input port is coupled to said first pulse output port of said single-phase pulse-width modulator; said second pulse input port is coupled to said second pulse output port of said single-phase pulse-width modulator;

wherein said power converters are synchronized by controlling said single-phase pulse-width modulator thereby equalizing the output currents from said current output ports.

2. The synchronized parallel running power converter according to claim 1 wherein said first power converter further comprises:

a first transistor whose drain terminal electrically is connected to a power source and gate terminal electrically is connected to said first pulse output port of said single-phase pulse-width modulator;

a second transistor whose drain terminal electrically is connected to the source terminal of said first transistor, whose source terminal electrically is connected to a ground, and whose gate terminal electrically connected to said second pulse output port of said pulse-width modulator; and

a first inductor coupled between said source terminal of said first transistor and said current output port of said first power converter.

3. The synchronized parallel running power converter according to claim 2 wherein said gate terminal of said first transistor is electrically connected to said first pulse output port of said single-phase pulse-width modulator through a first resister.

4. The synchronized parallel running power converter according to claim 2 wherein said gate terminal of said second transistor is electrically connected to said second pulse output port of said single-phase pulse-width modulator through a second resister.

5. The synchronized parallel running power converter according to claim 1 wherein said second power converter further comprises:

a third transistor whose drain terminal is electrically connected to a power source and gate terminal is electrically connected to said first pulse output port of said single-phase pulse-width modulator;

a fourth transistor whose drain terminal is electrically connected to the source terminal of said third transistor, whose source terminal is electrically connected to a ground, and whose gate terminal is electrically connected to said second pulse output port of said pulse-width modulator; and

a second inductor coupled between said source terminal of said third transistor and said current output port of said second power converter.

6. The synchronized parallel running power converter according to claim 5 wherein said gate terminal of said third transistor is electrically connected to said first pulse output port of said single-phase pulse-width modulator through a third resister.

7. The synchronized parallel running power converter according to claim 5 wherein said gate terminal of said fourth transistor is electrically connected to said second pulse output port of said single-phase pulse-width modulator through a fourth resister.

8. A synchronized parallel running power converter, controlled by a double-phase pulse-width modulator, said double-phase pulse-width modulator having a first pulse output port, a second pulse output port, a third pulse output port and a fourth pulse output port for pulse outputs, said power converter comprising:

a first power converter, having a first pulse input port, a second pulse input port and a current output port; said first pulse input port is coupled to said first pulse output port of said double-phase pulse-width modulator; said second pulse input port is coupled to said second pulse output port of said double -phase pulse-width modulator; and

a second power converter, having a first pulse input port, a second pulse input port and a current output port; said first pulse input port is coupled to said first pulse output port of said double-phase pulse-width modulator; said second pulse input port is coupled to said second pulse output port of said double-phase pulse-width modulator;

a third power converter, having a first pulse input port, a second pulse input port and a current output port; said first pulse input port is coupled to said third pulse output port of said double-phase pulse-width modulator; said second pulse input port is coupled to said fourth pulse output port of said double -phase pulse-width modulator; and

a fourth power converter, having a first pulse input port, a second pulse input port and a current output port; said first pulse input port is coupled to said third pulse output port of said double-phase pulse-width modulator; said second pulse input port is coupled to said fourth pulse output port of said double-phase pulse-width modulator;

wherein said power converters are synchronized by controlling said double-phase pulse-width modulator thereby equalizing the output currents from said current output ports.

9. The synchronized parallel running power converter according to claim 8 wherein said first power converter further comprises:

a first transistor whose drain terminal is electrically connected to a power source, and whose gate terminal is electrically connected to said first pulse output port of said double-

phase pulse-width modulator;

a second transistor whose drain terminal is electrically connected to the source terminal of said first transistor, whose source terminal is electrically connected to a ground, and whose gate terminal is electrically connected to said second pulse output port of said pulse-width modulator; and

a first inductor coupled between said source terminal of said first transistor and said current output port of said first power converter.

10. The synchronized parallel running power converter according to claim 9 wherein said gate terminal of said first transistor is electrically connected to said first pulse output port of said double-phase pulse-width modulator through a first resister.

11. The synchronized parallel running power converter according to claim 9 wherein said gate terminal of said second transistor is electrically connected to said second pulse output port of said double-phase pulse-width modulator through a second resister.

12. The synchronized parallel running power converter according to claim 8 wherein said second power converter further comprises:

a third transistor whose drain terminal is electrically connected to a power source, and whose gate terminal is electrically connected to said first pulse output port of said double-phase pulse-width modulator;

a fourth transistor whose drain terminal is electrically connected to the source terminal of said third transistor, whose source terminal is electrically connected to a ground, and whose gate terminal is electrically connected to said second pulse output port of said pulse-width modulator; and

a second inductor coupled between said source terminal of said third transistor and said current output port of said second power converter.

13. The synchronized parallel running power converter according to claim 12

wherein said gate terminal of said third transistor is electrically connected to said first pulse output port of said double-phase pulse-width modulator through a third resister.

14. The synchronized parallel running power converter according to claim 12 wherein said gate terminal of said fourth transistor is electrically connected to said second pulse output port of said double-phase pulse-width modulator through a fourth resister.

15. The synchronized parallel running power converter according to claim 8 wherein said third power converter further comprises:

a fifth transistor whose drain terminal is electrically connected to a power source, and whose gate terminal is electrically connected to said first pulse output port of said double-phase pulse-width modulator;

a sixth transistor whose drain terminal is electrically connected to a source terminal of said fifth transistor, whose source terminal is electrically connected to a ground, and gate terminal is electrically connected to said third pulse output port of said pulse-width modulator; and

a third inductor coupled between said source terminal of said fifth transistor and said current output port of said third power converter.

16. The synchronized parallel running power converter according to claim 15 wherein said gate terminal of said fifth transistor is electrically connected to said third pulse output port of said double-phase pulse-width modulator through a fifth resister.

17. The synchronized parallel running power converter according to claim 15 wherein said gate terminal of said sixth transistor is electrically connected to said fourth pulse output port of said double-phase pulse-width modulator through a sixth resister.

18. The synchronized parallel running power converter according to claim 8 wherein said fourth power converter further comprises:

a seventh transistor, whose drain terminal is electrically connected to a power source,

and whose gate terminal is electrically connected to said third pulse output port of said double-phase pulse-width modulator;

a eighth transistor whose drain terminal is electrically connected to a source terminal of said seventh transistor, whose source terminal is electrically connected to a ground, and gate terminal is electrically connected to said fourth pulse output port of said pulse-width modulator; and

a fourth inductor coupled between said source terminal of said seventh transistor and said current output port of said fourth power converter.

19. The synchronized parallel running power converter according to claim 18 wherein said gate terminal of said seventh transistor is electrically connected to said third pulse output port of said double-phase pulse-width modulator through a seventh resister.

20. The synchronized parallel running power converter according to claim 18 wherein said gate terminal of said eighth transistor is electrically connected to said fourth pulse output port of said double-phase pulse-width modulator through a eighth resister.